

## METHOD OF MANUFACTURING A SEMICONDUCTOR DEVICE

This application is based on Japanese patent application NO.2002-347094, the content of which is incorporated hereinto  
5 by reference.

## BACKGROUND OF THE INVENTION

## 1. Field of the Invention

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This invention relates to a method of manufacturing a semiconductor device. In particular, it relates to a method of manufacturing a semiconductor device comprising damascene interconnections.

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## 2. Description of the Related Art

Recently, copper having a lower specific resistance has been often used as a material for an interconnection in a  
20 semiconductor device. Since it is difficult to perform reactive ion etching on copper, the damascene process is usually employed for forming the interconnection when using copper as the interconnect material. Known damascene processes include a single damascene process in which an  
25 interconnection layer and a via hole are stepwise formed and a dual damascene process in which an interconnection layer

and a via hole are simultaneously formed. Among these, a dual damascene process, disclosed in JP-A No. 2002-203898 for example, is advantageous in the light of reduction in the number of steps because the via hole and the interconnection trench are simultaneously buried. The via hole may be made of the same type of copper as that for the interconnection to reduce a resistance of the via hole.

Forming an interconnection structure using a dual damascene process can be conducted by a via-first or trench-first process. In a via-first process, a via hole is first formed and an interconnection trench is then formed such that the trench is superposed over the via hole pattern. On the other hand, in a trench-first process, an interconnection trench is first formed and a via hole is then formed such that the via hole is superposed over the trench. The former is advantageous in the light of ensuring good contact performance of the via hole. Now referring to FIGS. 1A to 1D and 2A to 2D, conventional via-first steps of the dual damascene process will be described below.

FIG 1A shows the step in which a first interconnection 20 103, diffusion barrier film 105 and a second insulating film 107 are sequentially formed on a substrate (not shown in the drawings). After depositing a first insulating film 101 on the substrate, an interconnection trench is formed by dry etching and then a barrier metal film (not shown in the 25 drawings) and a copper film are formed in sequence such that

the trench is filled with them. Then, extraneous barrier metal and copper films formed outside of the interconnection trench are removed by CMP (Chemical Mechanical Polishing), to form the first interconnection 103. Next, on the first 5 interconnection 103 is formed the diffusion barrier film 105. The diffusion barrier film 105 is formed for preventing copper from diffusing into the insulating film and is also used as an etching stopper film during forming a via hole 111. Then, on the diffusion barrier film 105 is formed the second 10 insulating film 107.

The second insulating film 107 is an interlayer insulating film having a lower dielectric constant. Thus, the structure of FIG. 1A is provided.

Then, as shown in FIG. 1B, on the second insulating 15 film 107 are sequentially formed an anti-reflection film (not shown in the drawings) and a resist film 109, and a resist pattern for the via hole 111 is formed by lithography. Then, the via hole 111 is formed by dry etching. During the process, etching is stopped on the diffusion barrier film 105, 20 utilizing a difference in an etching rate between the second insulating film 107 and the diffusion barrier film 105 for preventing copper contamination due to exposure of the first interconnection 103, ashing after etching and damage to the copper during a washing procedure. After etching, the resist 25 film 109 and the anti-reflection film are removed by ashing.

Then, as shown in FIG. 1C, on the second insulating

film 107 are sequentially formed an anti-reflection film (not shown in the drawings) and a resist film 115, and then a resist pattern for the interconnection trench 117 is formed as described above. Then, the interconnection trench 117 is 5 formed by dry etching. During the process, the bottom of the via hole 111 is not etched because the anti-reflection film or the resist film 115 is buried.

Then, as shown in FIG. 1D, the resist film 115 and the anti-reflection film are removed by ashing. Next, as shown 10 in FIG. 2A, the diffusion barrier film 105 in the bottom of the via hole 111 is removed by dry etching to expose the first interconnection 103.

Then, as shown in FIG. 2B, a barrier metal film 119 and a copper film (not shown in the drawings) to be a seed layer 15 for electroplating are sequentially formed by sputtering over the whole surface of the second insulating film 107 including the via hole 111 and the interconnection trench 117. Subsequently, a copper film 121 is buried in the via hole 111 and the interconnection trench 117 by electroplating.

20 Then, as shown in FIGs. 2C and 2D, the extraneous copper film 121 and barrier metal film 119 are removed by CMP.

As described above, there are formed the copper film 121, i. e., the second interconnection in the interconnection trench 117, and the via hole connecting the first 25 interconnection 103 with the second interconnection.

## SUMMARY OF THE INVENTION

However, we have found a new problem after investigating the process shown in FIGS. 1A to 1D and 2A to 5 2D. Specifically, it has been found that during etching the diffusion barrier film 105 in the bottom of the via hole 111 in the process shown in FIG. 2A, etching is relatively faster in the corner of the second insulating film 107 in the upper part of the interconnection trench 117 so that the film is 10 etched in the form of a normal taper as shown in FIG. 2A. Thus, in an interval between fine interconnections, a distance in the upper part of the interconnection trench 117 is further reduced, causing a parasitic capacitance and also short circuit failure.

15 In view of the problems, an objective of this invention is to provide a method of manufacturing a semiconductor device in which a parasitic capacitance is inhibited between metal films such as interconnections, plugs and pads. Another object of this invention is to provide a method of 20 manufacturing a semiconductor device in which short circuit is inhibited between metal films such as interconnections, plugs and pads.

According to the present invention, there is provided a method of manufacturing a semiconductor device comprising:  
25 forming an insulating film on a semiconductor substrate, forming a concave in the insulating film and then forming a

metal film filling the concave; conducting a first polishing over the whole surface of the substrate to form a metal area filled in the concave; and conducting a second polishing over the whole surface of the substrate to remove parts of the 5 metal area and of the insulating film; wherein the second polishing also removes a part of the normal taper formed in the upper part of the concave.

According to the manufacturing method of this invention, the method comprises removing a part of the normal taper 10 formed in the upper part of the concave so that a parasitic capacitance or short circuit failure between metal areas can be prevented in the normal taper.

According to the present invention, there is provided a method of manufacturing a semiconductor device comprising: 15 forming an insulating film on a semiconductor substrate, forming a concave in the insulating film and then forming a metal film filling the concave; conducting a first polishing over the whole surface of the substrate to form a metal area filled in the concave; and conducting a second polishing over 20 the whole surface of the substrate to remove parts of the metal area and of the insulating film; wherein the second polishing also removes at least a part of the normal taper formed in the upper part of the concave.

For example, for a semiconductor device comprising a 25 lower interconnection on the substrate, the normal taper formed in the upper part of the concave before removing the

extraneous metal film is often formed during exposing the lower interconnection.

According to the present invention, there is provided a method of manufacturing a semiconductor device comprising:

- 5 forming a first interconnection of a metal film on a semiconductor substrate; forming an insulating film covering the first interconnection; selectively removing the insulating film to form a via hole reaching the upper surface of the first interconnection and an interconnection trench
- 10 connected to the via hole; forming a metal film filling the via hole and the interconnection trench; conducting a first polishing over the whole surface of the substrate to form a second interconnection filled in the via hole and the interconnection trench as well as a connection plug; and
- 15 conducting a second polishing over the whole surface of the substrate to remove parts of the second interconnection and of the insulating film; wherein the second polishing also removes at least a part of a normal taper formed in the upper part of the second interconnection trench.

- 20 The above method according to this invention comprises removing at least a part of the normal taper formed in the upper part of the interconnection trench so that a parasitic capacitance or short circuit failure between metal films filling the concave can be, therefore, also reliably and effectively prevented in a dual damascene process.
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According to the present invention, there is provided a

method of manufacturing a semiconductor device comprising:  
forming an insulating film on a semiconductor substrate;  
forming a sacrificial film on the insulating film; removing  
the sacrificial film and the insulating film in sequence to  
5 form a concave in the insulating film and then forming a  
metal film filling the concave; conducting a first polishing  
over the whole surface of the substrate to form a metal area  
filled in the concave; and conducting the second polishing  
over the whole surface of the substrate to remove parts of  
10 the metal area and of the insulating film; wherein the second  
polishing also remove the sacrificial film.

The above method according to this invention comprises  
forming the sacrificial film on the insulating film and then  
removing the sacrificial film so that the normal taper formed  
15 in the upper part of the concave can be reliably removed. A  
parasitic capacitance or short circuit failure between metal  
films filling the concave can be, therefore, reliably and  
effectively prevented.

In the methods of manufacturing a semiconductor device  
20 according to this invention, forming the concave in the  
insulating film may comprise conducting etching under the  
etching conditions in which the sacrificial film is more  
slowly etched than the insulating film. Etching under the  
above conditions can reduce a size of the taper formed in the  
25 upper part of the concave. Thus, it results in thinner  
polishing in the second polishing so that short circuit

failure between interconnections can be much more effectively prevented.

Etching conditions include, for example, the type of the insulating film, the type of an etching gas and a bias-  
5 voltage value. Specifically, when using an organic film as insulating film and a gas containing hydrogen and nitrogen as an etching gas, a material for a sacrificial film is preferably SiO<sub>2</sub> which is etching-resistant to the gas.

According to the present invention, there is provided a  
10 method of manufacturing a semiconductor device comprising:  
forming a first interconnection of a metal film on a semiconductor substrate; forming an insulating film such that it covers the first interconnection; forming a sacrificial film on the insulating film; selectively removing the  
15 insulating film and the sacrificial film in sequence to form a via hole reaching an upper surface of the first interconnection and an interconnection trench connected to the via hole; forming a metal film filling the via hole and the interconnection trench; conducting a first polishing over  
20 a whole surface of the substrate to form a second interconnection and a connection plug filled in the hole and the interconnection trench; and conducting a second polishing over the whole surface of the substrate to remove parts of the second interconnection and of the insulating film;  
25 wherein the second polishing also remove the sacrificial film on the insulating film.

In a dual damascene process, a parasitic capacitance or short circuit failure between metal films filling a concave can be reliably and effectively prevented by forming the sacrificial film on the insulating film and removing it.

5       In the method of manufacturing a semiconductor device according to this invention, removing at least a part of the normal taper formed in the upper part of the concave may be conducted before removing parts of the metal area and of the insulating film. Thus, the normal taper formed in the upper 10 part of the concave can be more reliably removed.

In the method of manufacturing a semiconductor device according to this invention, forming the via hole and the interconnection trench in the insulating film may comprise conducting etching under the etching conditions in which the 15 sacrificial film is more slowly etched than the insulating film.

Etching under the above conditions can reduce a size of the taper formed in the upper part of the interconnection trench. Thus, it results in thinner polishing in the second 20 polishing so that short circuit failure between interconnections can be much more effectively prevented.

In the method of manufacturing a semiconductor device according to this invention, an information on a polishing rate in the second polishing may be obtained and on the basis 25 of the information, the end point of the second polishing may be determined.

The manufacturing method according to this invention comprises obtaining information on a polishing rate in the second polishing and conducting polishing for a period determined on the basis of the information, so that a 5 polishing thickness can be controlled. Thus, the normal taper formed in the upper part of the concave can be more reliably removed.

In the method of manufacturing a semiconductor device according to this invention, a thickness of the insulating 10 film polished along with the metal area may be observed to determine the end point of the second polishing.

The manufacturing method according to this invention comprises conducting polishing while observing a thickness of the insulating film polished, so that a thickness of the 15 insulating film polished can be controlled. Thus, the normal taper formed in the upper part of the metal area can be further reliably removed.

This summary of the invention does not necessarily describe all necessary features so that the invention may 20 also be a sub-combination of these described features.

#### BRIEF DESCRIPTION OF THE DRAWINGS

FIGs. 1A to 1D are process cross sections illustrating 25 a process for manufacturing a semiconductor device of the related art.

FIGs. 2A to 2D are process cross sections illustrating a process for manufacturing a semiconductor device of the related art.

FIGs. 3A to 3D are process cross sections illustrating 5 a process for manufacturing a semiconductor device according to an embodiment of this invention.

FIGs. 4A to 4D are process cross sections illustrating a process for manufacturing a semiconductor device according to an embodiment of this invention.

10 FIGs. 5A to 5D are process cross sections illustrating a process for manufacturing a semiconductor device according to an embodiment of this invention.

FIGs. 6A to 6D are process cross sections illustrating 15 a process for manufacturing a semiconductor device according to an embodiment of this invention.

FIG. 7 illustrates a method for controlling a polishing thickness according to an embodiment of this invention.

FIG. 8 illustrates a method for controlling a polishing thickness according to an embodiment of this invention.

20 FIG. 9 illustrates a method for controlling a polishing thickness according to an embodiment of this invention.

#### DETAILED DESCRIPTION OF THE INVENTION

25 The invention will now be described based on the preferred embodiments. This does not intend to limit the

scope of the present invention, but exemplify the invention.

In these embodiments, polishing is conducted such that a taper formed in the upper part of the interconnection trench is removed, to prevent a parasitic capacitance or 5 short circuit failure between metal areas. Preferred embodiments will be described with reference to the drawings.

#### First Embodiment

FIGs. 3A to 3D and 4A to 4D are process cross sections 10 illustrating a process for manufacturing a semiconductor device according to this embodiment. FIG. 3A shows the step of forming a first insulating film 201, a first interconnection 203 in the first insulating film 201, a diffusion barrier film 205 and a second insulating film 207 15 on a substrate (not shown in the drawings) in sequence.

The structure in FIG. 3A is formed as described below. On a substrate is deposited a first insulating film 201 and an interconnection trench is formed by dry etching. Then, 20 barrier metal and copper films (not shown in the drawings) are sequentially formed such that the inside of the trench is filled with them. Then, the extraneous barrier metal and the copper films formed outside of the interconnection trench is removed by CMP to form a first interconnection 203. Next, on the first interconnection 203 is formed the diffusion barrier 25 film 205. The diffusion barrier film 205 is formed for preventing copper as a material for the first interconnection

203 from diffusing into the insulating film and for being used as an etching stopper film during formation of a via hole 211. On the diffusion barrier film 205 is formed a second insulating film 207. Thus, the structure in FIG. 3A  
5 is formed.

The first interconnection 203 may be made of Al, W or TiN in place of Cu. The diffusion barrier film 205 may be made of, for example, SiC or SiN. A thickness of the diffusion barrier film 205 is, for example, 25 nm to 100 nm  
10 both inclusive.

The second insulating film 207 is made of, for example, SiOC having a specific dielectric constant of 3.5 or less. SiOC is sometimes represented as SiOCH and generally contains Si, O, C and H as constituent elements. The second insulating film 207 may be formed by an appropriate method such as CVD. Other examples of a material which can be used include a variety of materials having a lower dielectric constant; for example, hydrogenated siloxane (HSQ), methylsiloxane (MSQ), hydrogenated methylsiloxane (MHSQ),  
15 polyimide (PI), perfluorocarbon (PFC), aromatic ether (PAE), aromatic hydrocarbon (PAHC) and benzocyclobutene (BCB) and their derivatives. A film made of any of these materials can be formed by an appropriate method such as CVD or spin coating. A thickness of the second insulating film 207 is,  
20 for example, 500 nm to 2000 nm both inclusive.

Next, as shown in FIG. 3B, on the second insulating

film 207 are sequentially formed an anti-reflection film (not shown in the drawings) and a resist film 209, and then a resist pattern for a via hole 211 is formed by lithography. Then, a via hole 211 is formed by dry etching. During the 5 process, etching is stopped on the diffusion barrier film 205, utilizing a difference in an etching rate between the second insulating film 207 and the diffusion barrier film 205 for preventing metal contamination due to exposure of the first interconnection 203, ashing after etching, and damage to the 10 metal during a washing procedure. After etching, the resist film 209 and the anti-reflection film are removed by ashing.

Then, as shown in FIG. 3C, on the second insulating film 207 are sequentially formed an anti-reflection film (not shown in the drawings) and a resist film 215, and then a 15 resist pattern for the interconnection trench 217 is formed as described above. Then, the interconnection trench 217 is formed by dry etching. During the process, the bottom of the via hole 211 is not etched because the anti-reflection film or the resist film 215 is buried.

20 Then, as shown in FIG. 3D, the resist film 215 and the anti-reflection film are removed by ashing. Next, as shown in FIG. 4A, the diffusion barrier film 205 in the bottom of the via hole 211 is removed to expose the first interconnection 203.

25 In the process, as shown in FIG. 4A, an etching rate in the upper part of the interconnection trench 217 is higher so

that the upper part of the interconnection trench 217 is etched in a form of a normal taper.

Then, as shown in FIG. 4B, a barrier metal film 219 and a copper film (not shown in the drawings) to be a seed layer 5 for electroplating are sequentially formed by sputtering over the whole surface of the second insulating film 207 including the via hole 211 and the interconnection trench 217. The barrier metal film 219 may be made of, for example, high melting metals or high melting metal compounds such as Ta, 10 TaN, TiN and TiSiN and a stack of these. A thickness of the barrier metal film 219 is, for example, 10 nm to 50 nm both inclusive.

Subsequently, a copper film 221 is simultaneously buried in the via hole 211 and the interconnection trench 217 15 by electroplating. The copper film 221 may be made of the same material as that for the first interconnection 203. A thickness of the copper film 221 is, for example, 300 nm to 2000 nm both inclusive.

Then, as shown in FIGS. 4C and 4D, the extraneous 20 copper film 221 and barrier metal film 219 formed in the area except the concave are removed by CMP to provide a semiconductor device in which the copper film 221 in the interconnection trench 217 is the second interconnection. The CMP process is conducted in two steps, i. e., the first 25 polishing where polishing is stopped on the surface of the barrier metal film 219 using a large polishing rate ratio

between the copper film 221 and the barrier metal film 219 (FIG. 4C)) and the second polishing where the remaining barrier metal film 219 is polished (FIG. 4D). In this embodiment, the second polishing polishes and flattens, along 5 with the barrier metal film 219, the second insulating film 207 and the copper film 221 in the taper formed in the upper part of the interconnection trench 217. Thus, a taper with a small interval between interconnections is removed so that even in a space between fine interconnections, short circuit 10 failure can be effectively prevented.

In the first polishing, a slurry is used, whereby the copper film 221 is efficiently polished. Such a slurry may contain, for example, an oxidizing agent such as H<sub>2</sub>O<sub>2</sub> and a corrosion inhibitor for a constituent metal in the copper 15 film 221.

In the second polishing, a slurry mainly for mechanical polishing is used for efficient polishing of the barrier metal film 219. Such a slurry may contain, for example, abrasive grains such as silica and a corrosion inhibitor for 20 a constituent in the copper film 221. Since the second insulating film 207 and the copper film 221 are polished along with the barrier metal film 219, a slurry with which a difference in a polishing rate between these films is small is used. It is preferable to use a slurry in which, for 25 example, a polishing rate ratio of the insulating film to the barrier metal is 1/3 to 3 both inclusive. Thus, dishing or

erosion can be prevented and the polished surface can be kept flat.

In the second polishing, all tapers in the upper part of the interconnection trench 217 may be polished or some of 5 the tapers may be polished as long as short circuit failure does not occur. Since a taper formed in the upper part of the interconnection trench 217 is often formed to a depth of about 50 nm or more when using a film having a lower dielectric constant such as SiOC as the second insulating 10 film 207, it is particularly effective to polish the second insulating film 207 to 50 nm or more from the upper surface in the second polishing for preventing a parasitic capacitance or short circuit failure.

Thus, in the manufacturing process of this embodiment, 15 a polishing thickness needs to be controlled for efficiently removing a taper in the second polishing. A controlling method will be described.

One of methods for controlling a polishing thickness is measurement of an interval between the upper surfaces of the 20 interconnection trenches 217. The method will be described with reference to FIG. 7. FIG. 7 is an enlarged view of the interval between upper part of the interconnection trench 217 in FIG. 4C.

On a dummy wafer is formed an interconnection pattern 25 in FIG. 4C as shown in FIGs. 3A to 3D and 4A to 4D. Then, varying a polishing time in the second polishing (the arrows

in FIG. 7), the interval between the upper surface of interconnection trench 217 in each stage is observed by, for example, SEM (scanning electron microscopy). CD-SEM is preferable because of more precise observation. The 5 polishing conditions can be set such that an interval width between the interconnection trenches 217 is measured and polishing is stopped when the width reaches a given value, to conveniently and efficiently control the thickness of the second insulating film 207 polished in the second polishing.

10 In setting the polishing conditions, an actual wafer may be used instead of a dummy wafer.

Alternatively, a polishing thickness can be controlled by a method where a light interference type of thickness meter placed in a CMP apparatus is used as a module for 15 detecting an end point as shown in FIG. 8. For example, a CMP apparatus, ISRM (in Situ Removal Monitor, from Applied Materials Inc.) may be used. In FIG. 8, in polishing pad 131 is formed a transparent window 133, into which a light enters. When a wafer 135 is above over the transparent window 133, a 20 light entering the transparent window 133 is reflected and from interference thus generated, a thickness of the insulating film in the surface of the wafer 135 can be determined. Employing such a configuration allows determination of a thickness when a barrier metal becomes 25 absent in each wafer 135 during CMP. Thus, a thickness of the second insulating film 207 to be polished can be

controlled by determining reduction in a thickness and then stopping polishing when the thickness is reduced to a given level.

5    Second Embodiment

FIGs. 5A to 5D and 6A to 6D show a process for manufacturing a semiconductor device according to this embodiment. The procedure to the configuration in FIG. 5A is as described in First Embodiment. FIG. 5A shows that a 10    sacrificial film 213 is formed on the upper surface of the second insulating film 207 in FIG. 3A.

The procedure in FIG. 5B and later is conducted as described in the procedure in FIG. 3B and later in First Embodiment to form a via hole 211 and an interconnection 15    trench 217, then, on a sacrificial film 213 including the interconnection trench 217 and the second insulating film 207, a barrier metal film 219 and a copper film 221 are formed. Thus, the cross section in FIG. 6B is provided.

Subsequently, as shown in FIGs. 6C and 6D, two-step CMP 20    is conducted as described in First Embodiment. In the second polishing, the barrier metal film 219 and the tapered sacrificial film 213, the copper film 221 are polished to remove the sacrificial film 213. A polishing level in the second polishing is controlled, for example, as described in 25    First Embodiment. Thus, the semiconductor device in FIG. 6D in which the copper film 221 in the interconnection trench

217 is the second interconnection.

A material for the sacrificial film 213 may be selected from those exhibiting an etching rate equal to or lower than that of the diffusion barrier film 205. A film exhibiting an etching rate lower than that of the diffusion barrier film 205 gives an etching rate lower than that of the second insulating film 207, so that formation of a taper in the upper part of the interconnection trench 217 can be prevented. For example, when using SiC as a material for the diffusion barrier film 205, a film exhibiting an etching rate equal to or lower than that of SiC, such as SiO<sub>2</sub>, SiN, SiC, SiON and SiCN, can be used. A thickness of the sacrificial film 213 is, for example, 10 nm to 100 nm both inclusive. The film with a thickness of 10 nm or more can suitably prevent taper formation in the upper part of the interconnection trench 217 and thus can reduce a taper size. Furthermore, the film with a thickness of 100 nm or less can be efficiently removed in CMP.

Thus, in this embodiment, the sacrificial film 213 exhibiting an etching rate lower than that of the second insulating film 207 is formed on the second insulating film 207, so that etching of the corner can be prevented in the upper part of the interconnection trench 217. A taper size formed in the upper part of the interconnection trench 217 can be reduced in comparison with the case where a sacrificial film 213 is not formed. Therefore, as shown in

FIG. 9, a polishing level in the second polishing can be reduced in comparison with the case in FIG. 7, for example, 30 nm. FIG. 9 is an enlarged view of the interval between the upper part of the interconnection trench 217 in FIG. 6C.

5       Thus, in this embodiment, the sacrificial film 213 is formed on the second insulating film 207, to more efficiently remove the taper in the upper part of the interconnection trench 217. Short circuit between interconnections can be, therefore, more effectively prevented. Furthermore, since  
10      the sacrificial film 213 is removed by CMP, it is not necessary to take detachment from the second insulating film 207 into account. Thus, we can focus on performance as a sacrificial film 213, resulting in higher freedom in material selection.

15       Although the present invention has been described by way of exemplary embodiments, it should be understood that many changes and substitutions may be made by those skilled in the art without departing from the spirit and the scope of the present invention which is defined only by the appended  
20      claims.